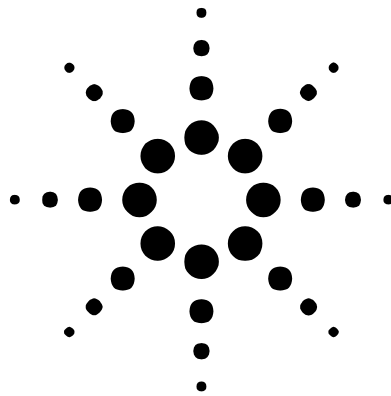




**Agilent Technologies**  
Innovating the HP Way

# Performance Verification Test Tool for 81200 Platform



## User Guide

Revision 1.0



## **1 Introduction**

### **1.1 Tasks of PVT**

The PVT is a software tool to conduct the Performance Verification Test (PVT) for the 81200 platform, that currently comprises the systems 81210 (previously 81200) and 81250. The systems are VXI-based and consist of clock and carrier modules, plug-in front-ends, and mainframes. The PVT tool needs to verify product functionality and specifications.

### **1.2 Requirements of PVT**

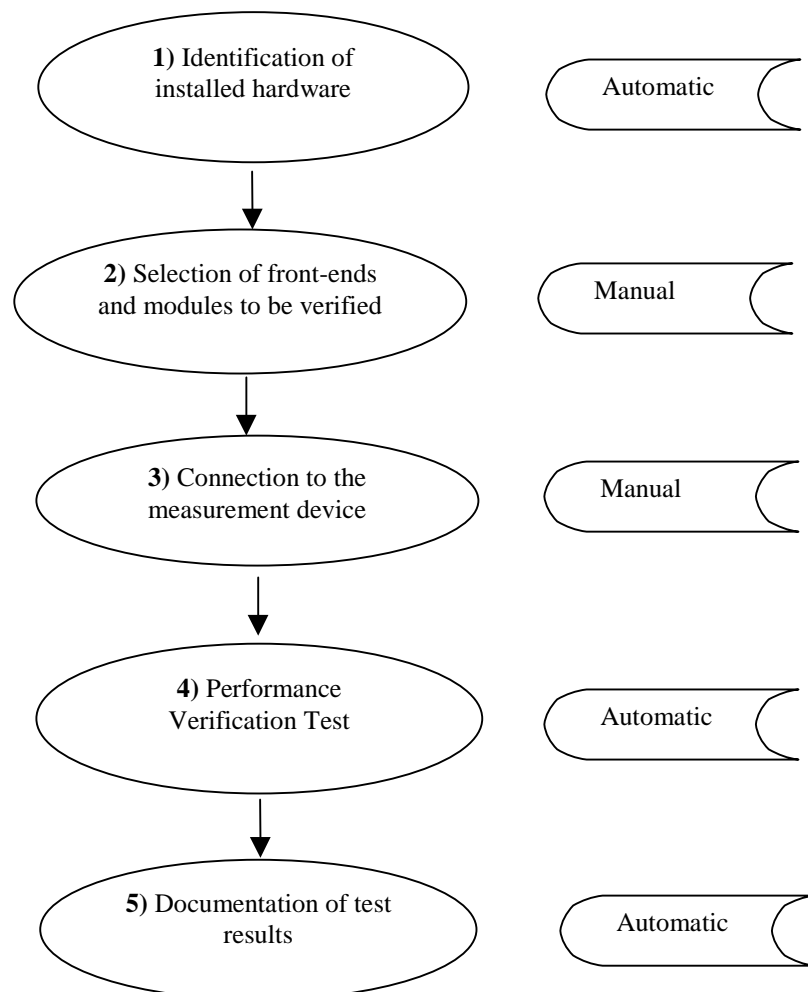
The PVT software tool will be used by service engineers at a customer-site or in local service centers of Agilent Technologies for fast support, e.g. repair or calibration.

The aim of the PVT tool is to provide field service a semi-automatic program procedure to verify multiple Data channels.

The PVT Tool is built upon the TEST EXEC SL. It is possible to set up an individual schedule of available test cycles

### **1.3 Software Structure**

#### 1.3.1 Simplified overview of program functionality



#### 1.3.1.1 Identification of installed hardware

The registration of the installed hardware will be displayed in a single overview on the Graphical User Interface (GUI). There, all modules installed are described with any front-ends they might contain and the front-ends addresses. Module and front-end slots not used are also displayed.

#### 1.3.1.2 Selection of front-ends and modules

The user of the PVT tool can select every front-end in the module that he wants to be tested. All possible performance verification test routines for the specific front-end/module is displayed and can be selected individually.

#### 1.3.1.3 Connection to the measurement device

After selecting the front-end and the verification test to be conducted, the user needs to connect the front-end to the measuring device manually. The PVT provide information about the required connections.

#### 1.3.1.4 Performance Verification Test

The PVT Software Tool conducts the complete Performance Verification Test in steps, e.g. by testing all front-end/carrier-module tests sequentially. In order to conduct the PVT steps, the Software Tool automatically will set all parameters for a selected front-end/module combinations.

After running each Performance Verification Test step, the user can repeat the step once more or proceed to the next step.

All settings for the measurement device, e.g. Oscilloscope, Counter or Digital Voltmeter, will be set automatically.

#### 1.3.1.5 Documentation of test results

User-selectable, all results can be displayed or printed out after each single Performance Verification Test step, or after finishing the complete Performance Verification Test. The Performance Verification Test results need to comprise the results measured and the specification values, also "Pass" or "Fail" needs to be indicated for each parameter.

## **2 PVT Software Tool Scope and Technical Requirements**

### **2.1 Scope**

The following tests for Modules and Generator and Analyzer front-ends can be performed:

#### Clock Modules:

1. System Clock
2. Clock Jitter

#### Generator front-ends:

1. Generator Delay
2. Generator Width
3. Generator Level
4. Generator Transition time
5. Generator Overshoot




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Analyzer front-ends:

1. Receiver Threshold

## 2.2 *Devices-under-Test*

Three systems have to be characterized:

- 81200 “Basic”
- 81210 “Basic” (successor of 81200)
- 81250 “ParBert” (CPL Apr 1 2000)

Each system supports a choice of different front-ends and modules:

### 81200 - System

Modules:

|        |  |
|--------|--|
| E4831A | Clock and Data Generator Module                  |
| E4841A | Module for Data Generator and Analyzer front-end |
| E4805A | Clock Module                                     |

Generator front-ends:

|        |                              |
|--------|------------------------------|
| E4842A | 330MHz (Differential Output) |
| E4843A | 660MHz (Differential Output) |
| E4846A | 200Mbit/s; Dual Output       |
| E4838A | 660MHz (Differential Output) |

Analyzer front-ends:

|        |                                       |
|--------|---------------------------------------|
| E4844A | 660MSa/s (Single Input)               |
| E4845A | 330MSa/s (Dual Input)                 |
| E4847A | 330MSa/s (Dual Input, High Impedance) |
| E4837A | 660MSa/s                              |

### 81210 – System

Modules

|        |  |
|--------|--|
| E4805B | Central Clock Modul  |
| E4831A | Clock and Data Generator Module                            |
| E4832A | Module for Data Generator and Analyzer front-end (660MHz)  |
| E4841A | Module for Data Generator and Analyzer front-end (660MHz)  |
| E4861A | Module for Data Generator and Analyzer front-end (2,6GB/s) |

Generator front-ends:

|        |                              |
|--------|------------------------------|
| E4838A | 660MHz (Differential Output) |
| E4843A | 660MHz                       |
| E4846A | 200Mbit/s; Dual Output       |
| E4862A | 2,6GSa/s                     |
| E4864A | 1,3GSa/s                     |

Analyzer front-ends:

|        |                                       |
|--------|---------------------------------------|
| E4835A | 660MSa/s                              |
| E4863A | 2,6GSa/s                              |
| E4865A | 1,3GSa/s                              |
| E4847A | 330MSa/s (Dual Input, High Impedance) |
| E4837A | 660MSa/s                              |
| E4844A | 660MSa/s (Single Input)               |
| E4845A | 330MSa/s (Dual Input)                 |



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## 81250 – System

### Modules

|        |  |
|--------|--|
| E4805B | Central Clock Modul  |
| E4832A | Module for Data Generator and Analyzer front-end (660MHz)  |
| E4861A | Module for Data Generator and Analyzer front-end (2,6GB/s) |

### Generator front-ends:

|        |                              |
|--------|------------------------------|
| E4838A | 660MHz (Differential Output) |
| E4843A | 660MHz                       |
| E4862A | 2,6GSa/s                     |
| E4864A | 1,3GSa/s                     |

### Analyzer front-ends:

|        |          |
|--------|----------|
| E4835A | 660MSa/s |
| E4863A | 2,6GSa/s |
| E4865A | 1,3GSa/s |

## 2.3 Measurement Equipment

### Recommended Devices.

- Oscilloscope with bandwidth >20GHz (e.g.: Agilent 54120, and 86100 series)
- Counter with range up to 1GHz (e.g. Agilent 53132A)
- Digital Volt Meter with a dc voltage range up to 10 V (e.g.: Agilent 34401A)

### Recommended Accessories:

- Attenuator 20db  
(Agilent 8493A, Opt.020)
- 4 SMA Cables á 50 Ohm **90cm length**  
(Agilent 8120-4948)
- Power Splitter 50Ohm  
(Agilent 11667B)
- 50 Ohm Feedthrough Termination, 10 W, 0.1 %
- Torque Wrench  
(Agilent 8710-1582)

## 2.4 Compatibilities

The Performance Verification Test Tool can test multiple numbers of one Module type with different Front-end combinations within a test cycle.

Every Module type needs to be tested individually:

E4841A, E4832A and E4861A.

We recommend to test clock group wise. This requires to test all Modules related to a common Clock Module to test in the same test cycle.

This will give the customer the best performance verification results, because all settings and specifications are depend on Clock Module, Data Module and Front-end.

To conduct a Performance Verification Test for a single Front-end or Data Module requires all HW Clock Module, Data Module to set up a proper system to run a complete test cycle.



### **3 How do I set up the PVT Tool**

- 1) You need to load the Test Exec SL and the PVT SW under different directories.  
Filename for the Test EXEC SL:  
    C:\Test EXEC SL  
Filename for the PVT User SW:  
    C:\PVT
  
- 2) Create an Start Icon for starting the Test EXEC SL. You will find the start icon under:  
    C:\Test Exec SL\bin\tstexecsl.exe  
In the shortcut properties please adjust following path in START IN:  
    C:\PVT\bin\
  
- 3) If necessary, you need to adjust the tstexecsl.ini with following paths:  
    Developer=C:\PVT\Bin\opui.dll  
    Operator=\$ROOT\$\bin\opui.dll  
    [Action Definition Paths]  
    Path00= C:\PVT \TestExec\Actions  
    [Dynamic Link Library Paths]  
    Path00= C:\PVT \Project Files\Bin  
    [Symbol Table Paths]  
    Path00= C:\PVT \TestExec\Symbols  
    [Topology Layer Paths]  
    Path00= C:\PVT\TestExec\Topology
  
- 4) By double clicking on the Test EXEC SL Button a small window will pop up  
Please do enter User name: WILD, no Password is necessary,  
and choose in the next window "Developer".

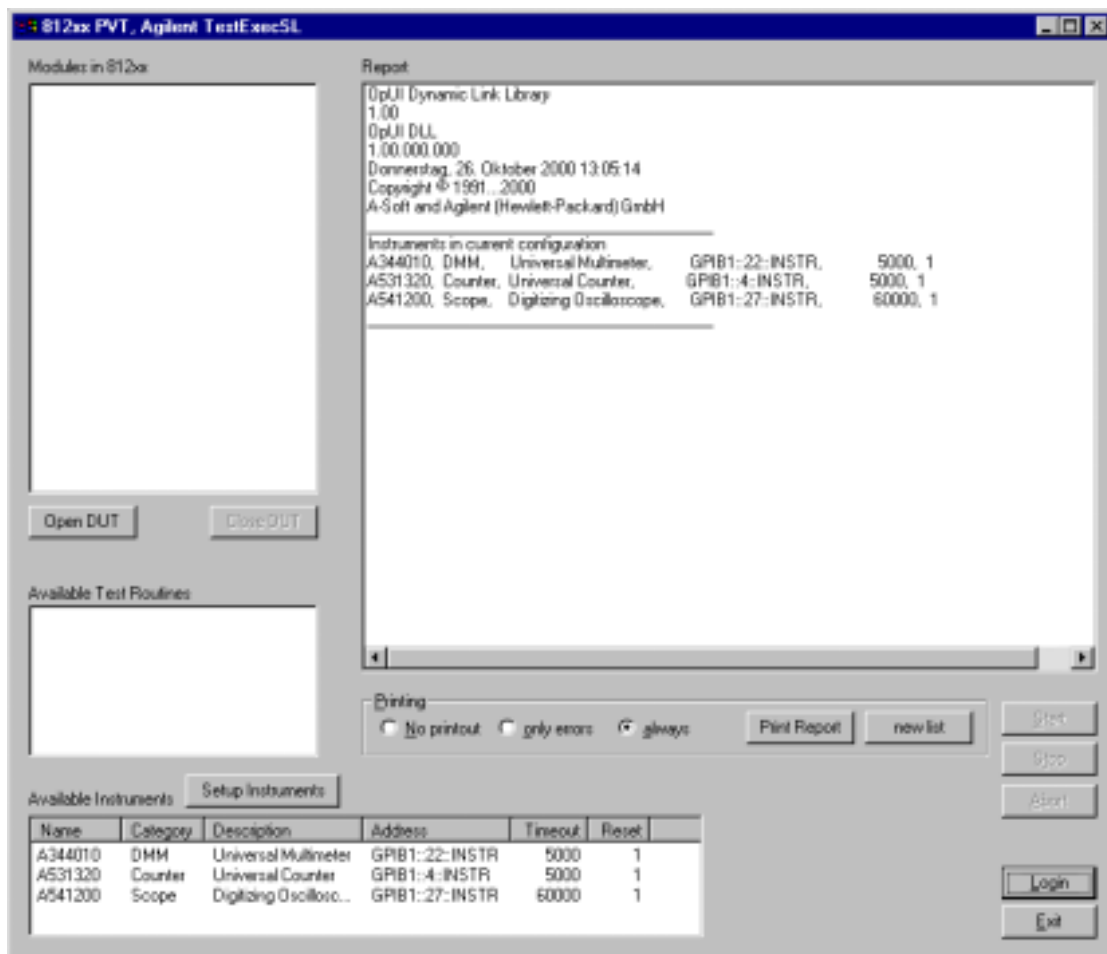
The Use Userinterface will pop up next as you will see in the next chapter.

### **4 Deskew Procedure**

Before running the Performance Verification Procedure the user must do a deskewing of each channel. Therefore it is necessary to have a known delay of the used cable. Please do following the Deskew Procedure in the User Manuel of the 812xx Software.



## 5 Structure of the user Interface



**Figure 1** User Interface of PVT

Figure 1 shows the User Interface of the PVT, there are four windows:

**-Modules in 812xx**

In the window "Modules in 812xx" there will be all detected front-ends displayed there you can select the front-end you want to test.

**-Report**

The report window will display all necessary information about the test report. The test report must be reviewed and the results of every verification procedure must be transferred into the report file of the attached document.

**-Available test Routines**

By selecting a front-end all available test routines for this front-end will be displayed and can be started separate. A test routine can multiple times running.

**-Available Instruments**

In this window, the user need to setup his measurement devices.



## 5.1 Step I

By pressing the "open DUT" button the user has got three choices:

81200, this does include front-ends within the E4841A module

81210, this test is currently the same as under 81250

81250, this test covers all front-ends which belongs to the modules E4832A and E4861A.

It is required that all module types are running separately and cannot mixed within one Hardware configuration.

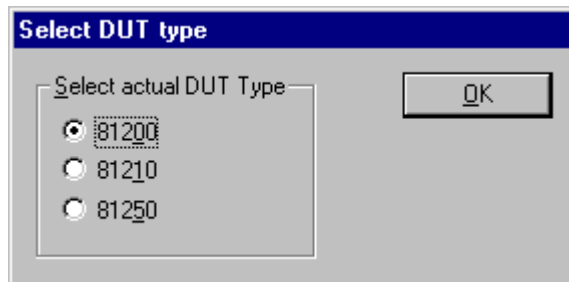


Figure 2: Select DUT Type

## 5.2 Step II

The next step after selecting the DUT type the Report window will show all modules, front-ends and clockboards installed in the current hardware configuration.

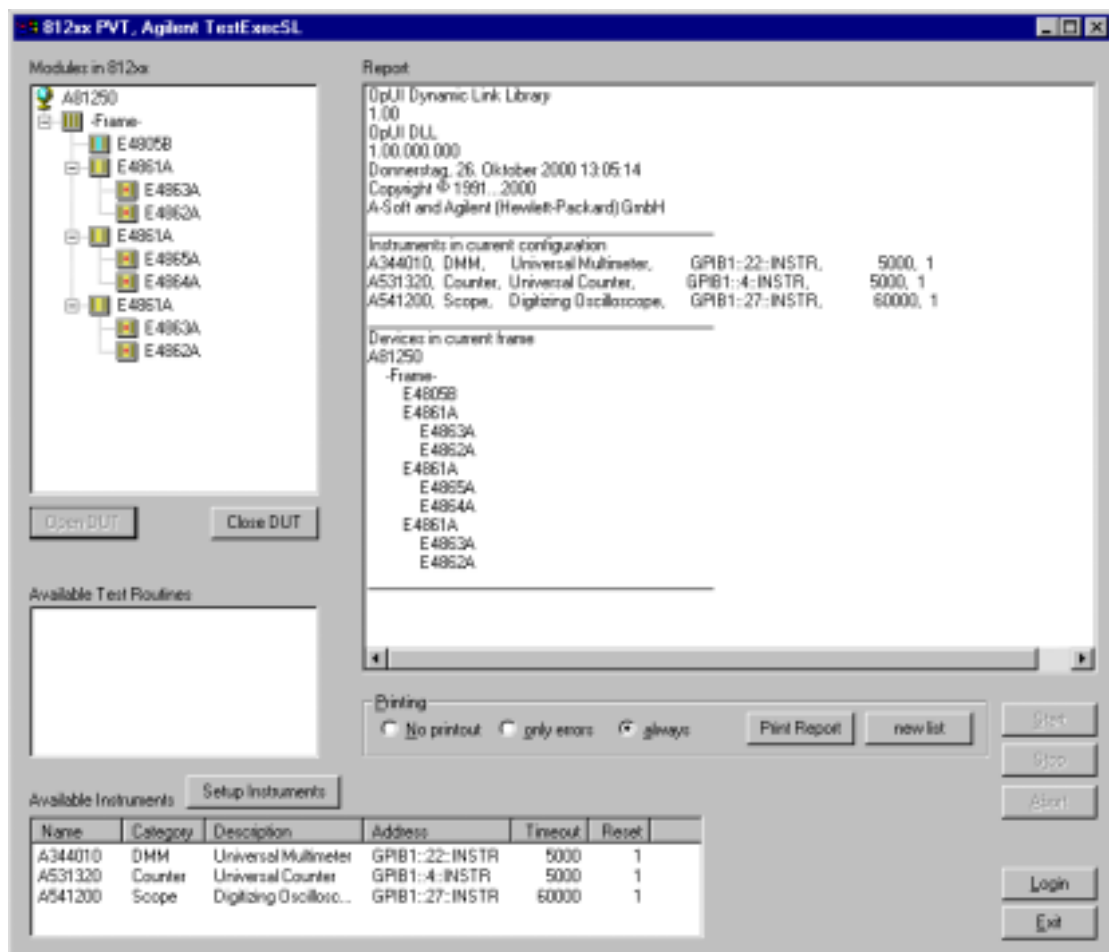


Figure 3: User Interface with hardware configuration





### 5.3 Step III

When selecting the front-end that needs to be tested, the window " Available Test Routines" will show all available test routines.

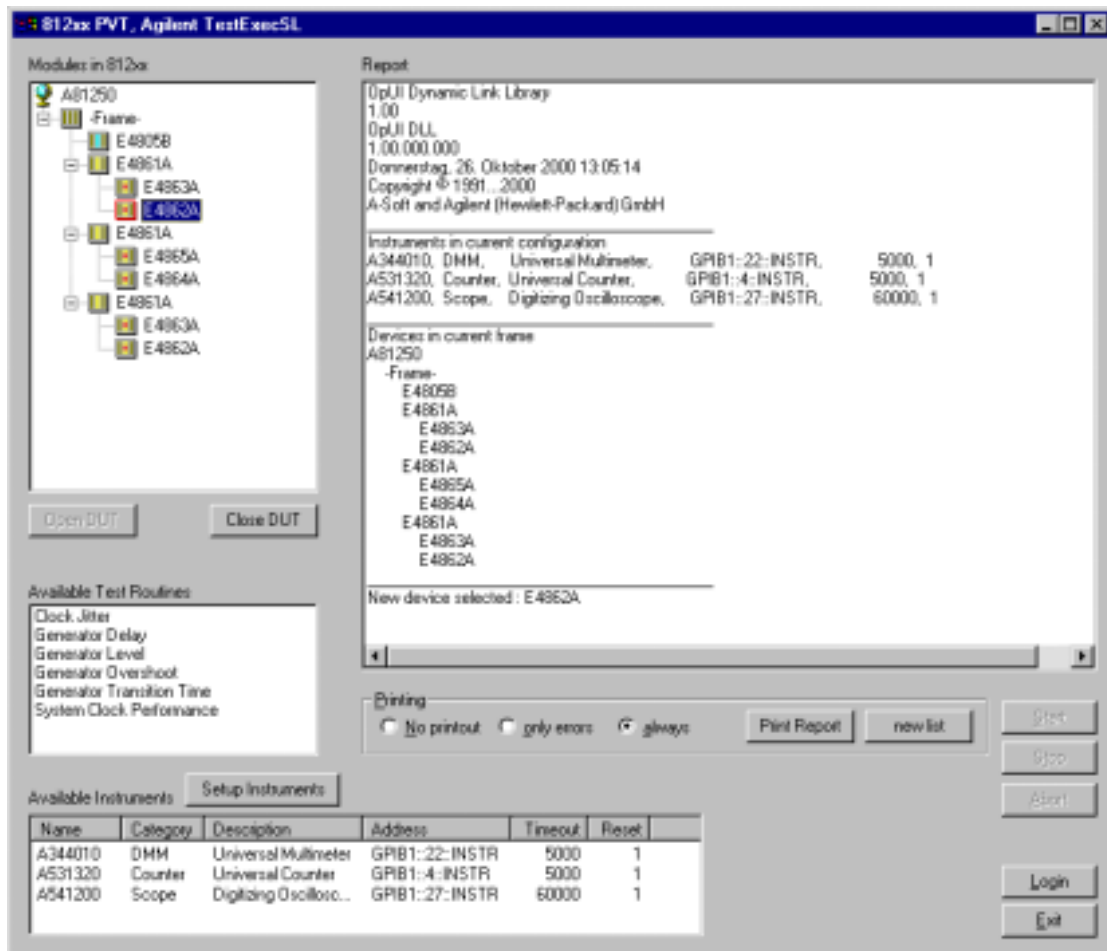


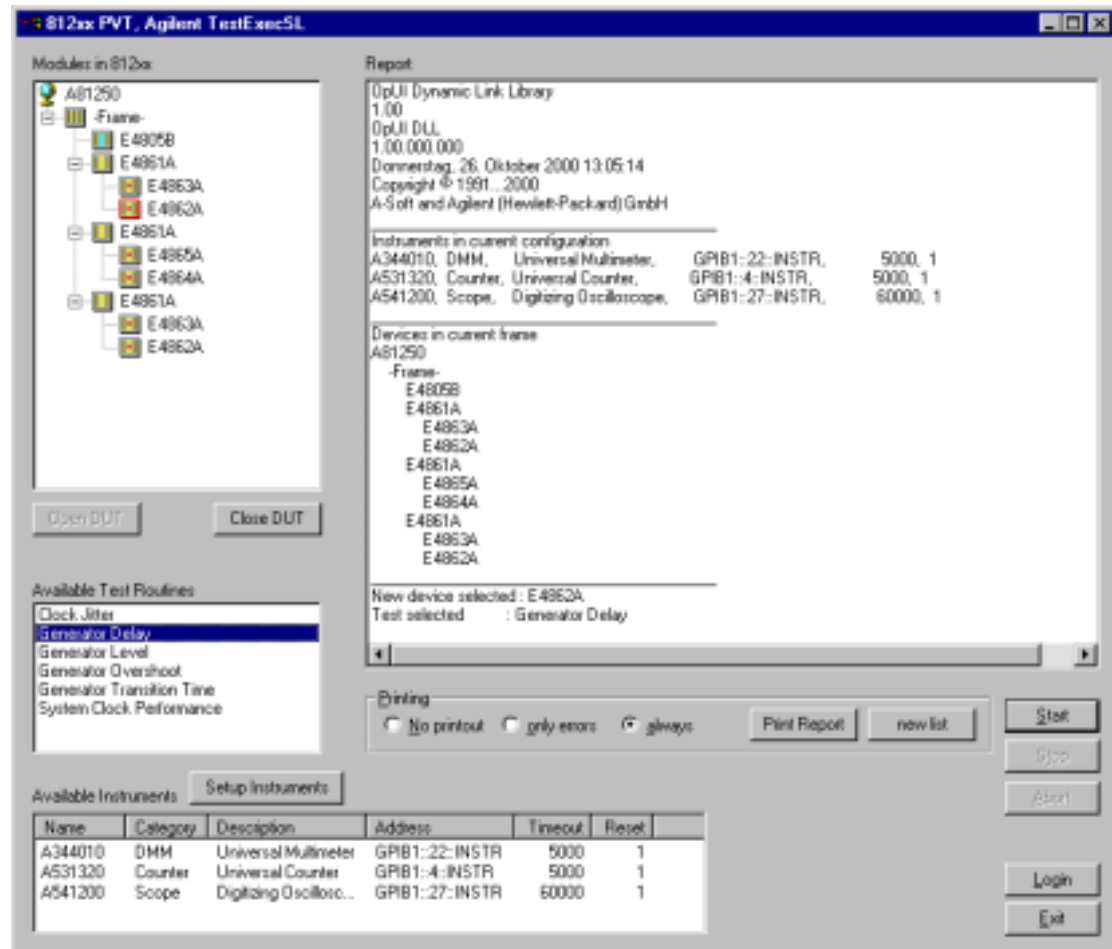
Figure 4 User Interface with available Test Routines



## 5.4 Step IV

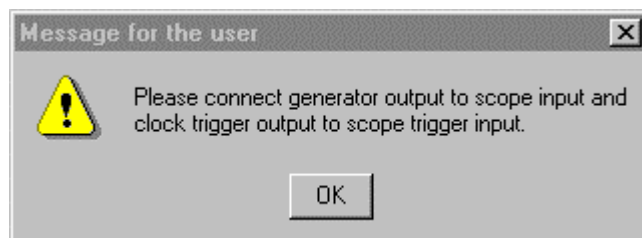
To select the test routine, the user needs to select the test routine. In the report window the name of the selected test routine will be display.

Second, you need to run the test routine by pressing the start button.



**Figure 5 Selected Test Routine**

Before the test routine will start, the user will be noticed to make all necessary connections. Please be aware, to use 20db Attenuators for scope input and scope trigger input.



**Figure 6 Information about connection**



## 5.5 Step V

After a test routine has finished, the result will be displayed in the report window.

The report window will also decide, whether the verification test was pass or fail.

BUT, you need to adapt the results into the PVT procedure and decide about the test result.

This is necessary, because there are many tests who cover a functionality or a typically specification.

A typically specification is whether pass nor fail, it must be decided by the user. A general answer what is fail or pass is, if the result is +/-20% of the typical specified value the test result can be seen as fail.

The screenshot shows the Agilent TestExec5L software interface. The main window is titled "812xx PVT, Agilent TestExec5L". It is divided into several sections:

- Modules in 812xx:** A tree view showing a hierarchy of modules: A81250, Frame, E4805B, E4861A, E4863A, E4862A, E4861A, E4865A, E4864A, E4861A, E4863A, and E4862A.
- Report:** A text area displaying test details:
  - Instruments in current configuration:
 

|  |                 |          |
|--|-----------------|----------|
| A344010, DMM, Universal Multimeter,      | GP1B1:22-INSTR, | 5000, 1  |
| A531320, Counter, Universal Counter,     | GP1B1:4-INSTR,  | 5000, 1  |
| A541200, Scope, Digitizing Oscilloscope, | GP1B1:27-INSTR, | 60000, 1 |
  - Devices in current frame:
    - A81250
    - Frame-
    - E4805B
    - E4861A
    - E4863A
    - E4862A
    - E4861A
    - E4865A
    - E4864A
    - E4861A
    - E4863A
    - E4862A
  - New device selected: E4862A
  - Test selected: Generator Delay
  - Testplan: A81250.E4862A.Generator Delay.tpa
  - Time: Donnerstag, 26. Oktober 2000, 13:10:03
  - Generator Delay: NDT OK
  - Generator Delay: 9.9485e-009 1.00905e-008
  - 4.056e-009 3.00417e-006
  - Execution time: 0:00:00.49
- Available Test Routines:** A list of test routines including Clock Jitter, Generator Delay (highlighted), Generator Level, Generator Overshoot, Generator Transition Time, and System Clock Performance.
- Available Instruments:** A table listing instruments:
 

| Name    | Category | Description          | Address        | Timeout | Reset |
|---------|----------|----------------------|----------------|---------|-------|
| A344010 | DMM      | Universal Multimeter | GP1B1:22-INSTR | 5000    | 1     |
| A531320 | Counter  | Universal Counter    | GP1B1:4-INSTR  | 5000    | 1     |
| A541200 | Scope    | Digitizing Oscill... | GP1B1:27-INSTR | 60000   | 1     |
- Printing:** Radio buttons for "No printout", "only errors", and "always" (selected). Buttons for "Print Report" and "new list".
- Buttons:** "Open DUT", "Close DUT", "Start", "Stop", "Abort", "Login", and "Exit".

Figure 7 Displayed results after performance test

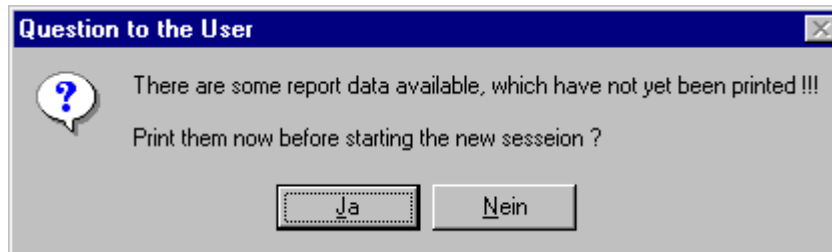


## 5.6 Step VI

The user has got the choice of printing the report to the current default printer.

The user can select between test results who cover " only errors" or "always" which will printout all results.

With the button "new List" a new report list will be generated and all previous test results in the report window are deleted.



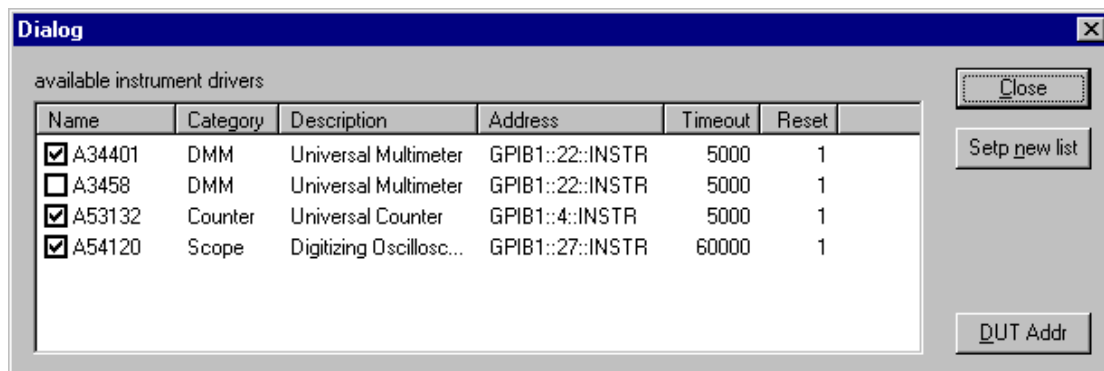
**Figure 8 Print out of data report**

## 6 PVT configuration

With "Setup Instruments" the user will be able to adapt the connected instruments via GPIB.

1. Mark the checkbox
2. Double click the device
3. Figure 11 will pop up

After adjusting the properties of the device, please press Setup new list and the new devices will be setup.



**Figure 9 Available instrument driver**



There are two possibilities for setting up the test environment and control the embedded PC:

A) Controlled via LAN from an external PC:

the User Software of the 812xx and the LAN Server must run on the embedded PC

the Test EXEC SL must run on the external PC

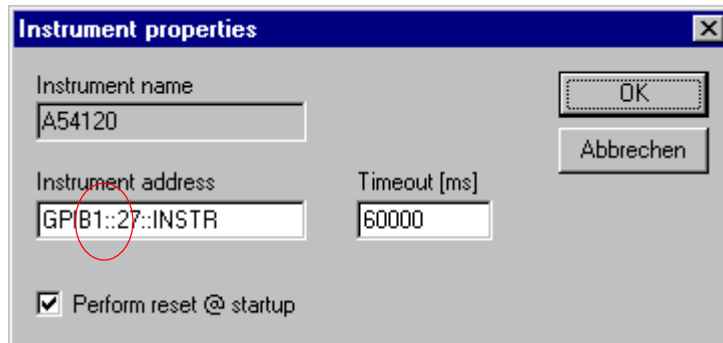
Please set up at Run I/O config at the WIN NT environment GPIB1

B) Working from the embedded PC:

the User Software and the Test EXEC SL must run on the embedded PC

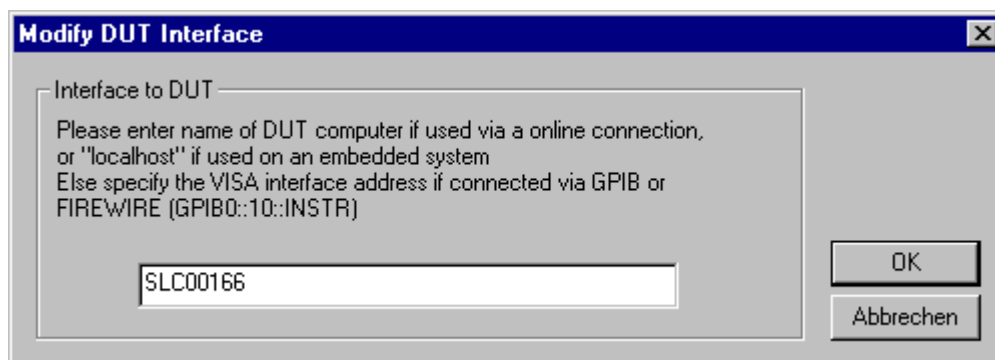
Please set up at RUN I/O config at the WIN NT environment GPIB0

The GPIB1 or GPIB0 must also be adapted in this window.



**Figure 10 Instrument Properties**

At the Setup Instrument window you need to modify the DUT address.  
This is the computer name where the User Software 812xx is running  
e.g.: BVSTP031



**Figure 11 Modify Computer name**



## 7 Report of the PVT tool

OpUI Dynamic Link Library

1.00

812xx OpUI DLL

1.03.000.000

Thursday, November 23, 2000 02:44:14 PM

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no additional specs

Main user interface

---

Instruments in current configuration

A344010, DMM, Universal Multimeter, GPIB1::22::INSTR, 5000, 1

A531320, Counter, Universal Counter, GPIB1::4::INSTR, 5000, 1

A541200, Scope, Digitizing Oscilloscope, GPIB1::7::INSTR, 5000, 1

---

Devices in current frame

A81200

-Frame-

E4805A

E4841A

-empty-

E4837A

E4843A

E4838A

---

Test selected : Clock Jitter

Testplan : A81200.E4838A.Clock Jitter.tpa

Time : Friday, November 24, 2000, 7:21:58 AM

Clock Jitter

Clock Jitter : Pass

1e-011

Specification: value must be <10ps typ

4.48333e-012

Measured value

Execution time : 0.00:01:37

---

Test selected : Generator Delay

Testplan : A81200.E4838A.Generator Delay.tpa

Time : Friday, November 24, 2000, 7:24:40 AM

Generator Delay

Generator Delay : Pass

9.9495e-009 1.00505e-008

Specifications: minimum - maximum value

9.99e-009 3.01002e-006

Measured value, functionality of 3000ns test

Execution time : 0.00:00:24

---

Test selected : Generator Overshoot

Testplan : A81200.E4838A.Generator Overshoot.tpa

Time : Friday, November 24, 2000, 7:25:09 AM

Generator Overshoot

Generator Overshoot : Pass

0.056 0.0375

Specification: value must be <56mV; measured value

Execution time : 0.00:00:12



Test selected : Generator Transition Time

Testplan : A81200.E4838A.Generator Transition Time.tpa

Time : Friday, November 24, 2000, 7:25:25 AM

Generator Transition Time

Generator Transition Time : Pass

5.5e-010 3.474e-010

Specification value; measured value

3.75e-010 6.25e-010 5.058e-010

Specification minimum - maximum value; measured value

4.65e-009 5.35e-009 4.9048e-009

Specification minimum - maximum value; measured value

Execution time : 0.00:00:37

Test selected : Generator Width

Testplan : A81200.E4838A.Generator Width.tpa

Time : Friday, November 24, 2000, 7:26:10 AM

Generator Width

Generator Width : Pass

4.975e-008 5.025e-008 5.00826e-008

Specification minimum - maximum value; measured value

9.79e-009 1.021e-008 9.9954e-009

Specification minimum - maximum value; measured value

Execution time : 0.00:00:29

Test selected : Generator Level

Testplan : A81200.E4838A.Generator Level.tpa

Time : Friday, November 24, 2000, 7:27:32 AM

Generator Level

Generator Level : Pass

-0.871 -0.929 -0.8895

Specification minimum - maximum value; measured value

4.248 4.552 4.3865

Specification minimum - maximum value; measured value

Execution time : 0.00:00:08

New device selected : E4838A

Test selected : System Clock Performance

Testplan : A81200.E4838A.System Clock Performance.tpa

Time : Friday, November 24, 2000, 7:51:32 AM

System Clock Performance

System Clock Performance : Pass

999.95 1000.05 1000.02

Specification minimum - maximum value; measured value

6.59967e+008 6.60033e+008 6.59998e+008

Specification minimum - maximum value; measured value

Execution time : 0.00:00:06



## **8 Documentation**

Agilent 81200 System: Performance Test Record

Page 1 of \_\_

Test Facility:

\_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

Report No.

\_\_\_\_\_

Date

\_\_\_\_\_

Customer

\_\_\_\_\_

Tested by

\_\_\_\_\_

Software Rev.

\_\_\_\_\_

Ambient temperature

\_\_\_\_\_

°C

Options

\_\_\_\_\_

Relative humidity

\_\_\_\_\_

%

System Configuration of the Agilent 81200 Data Generator / Analyzer Platform:

Mono-Frame System

If so :

Agilent E4840A  
Mainframe

Agilent E4849A/B/C  
Mainframe

Multi-Frame System

If so :

1 Extender Frame (Agilent  
E4848A/B)

2 Extender Frames (Agilent  
E4848A/B)





Mainframe Configuration:

| Slot No. | System Component                | Y/N | Model No.      | Serial No. |
|----------|---------------------------------|-----|----------------|------------|
|          | VXI MXI Interface Board         |     | Agilent E1482B |            |
|          | Central Board                   |     |                |            |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |
|          | Generator/Analyzer Module Board |     | Agilent E4841A |            |
|          | Front-Ends:                     | 1:  | 2:             | 3:         |











## Test 5: Generator Level:

|        | Digital Voltmeter | Specification  | Pass/Fail |
|--------|-------------------|----------------|-----------|
| E4838A |                   | 4,4V +/-152mV  | P / F     |
|        |                   | -0,9V +/- 29mV | P / F     |
| E4842A |                   | 3,5V +/-205mV  | P / F     |
|        |                   | -0,9V +/-127mV | P / F     |
| E4843A |                   | 3V +/-190mV    | P / F     |
|        |                   | -0,9V +/-127mV | P / F     |
| E4846A |                   | 2,5V +/-225mV  | P / F     |
|        |                   | -0,9V +/-145mV | P / F     |

## Test 6: Generator Transition Time:

|        | Oscilloscope reading | Specification            | Pass/Fail            |
|--------|----------------------|--------------------------|----------------------|
| E4838A |                      | 0,5ns@2,5V<br>+/-125ps   | P / F                |
|        |                      | 0,5ns @ 2,5V<br>+/-350ps | P / F                |
|        |                      | @ECL<br>350ps            | Functionality<br>P/F |
| E4842A |                      | 0,7ns@2,5V<br>+/-270ps   | P / F                |
|        |                      | 5ns @ 2,5V<br>+/-800ps   | P / F                |
|        |                      | @ECL<br><600ps           | P / F                |
| E4843A |                      | @ 2,5V<br>500ps          | Functionality<br>P/F |
|        |                      | @ 2,5V<br>500ps          | Functionality<br>P/F |
|        |                      | @ ECL<br><350ps          | Functionality<br>P/F |
| E4846A |                      | @ 2,5V<br><2,5ns         | Functionality<br>P/F |
|        |                      | @ 2,5V<br><2,5ns         | Functionality<br>P/F |
|        |                      | @ ECL<br><1,2ns          | Functionality<br>P/F |

## Test 7: Generator Overshoot

|        | Oscilloscope reading | Specification  | Pass/Fail              |
|--------|----------------------|----------------|------------------------|
| E4838A |                      | @ECL<br><56mV  | Functionality<br>P / F |
| E4842A |                      | @ECL<br><140mV | P / F                  |
| E4843A |                      | @ECL<br><40mV  | Functionality<br>P / F |
| E4846A |                      | @ECL<br><160mV | P / F                  |



**Central Board Tests, Test 8:**

Type of Front-end Module:  Agilent E4842A     Agilent E4843A     Agilent E4846A  
 Agilent E4838A

Location of host Agilent E4841A Module:  Mainframe    Position within Agilent E4841A Module:  1  
 Extender Frame 1     2  
 Extender Frame 2     3  
 4

Slot No. of host Agilent E4841A Module: \_\_\_\_\_

Serial No. of host Agilent E4841A Module: \_\_\_\_\_

**Test 8: Receiver Threshold Range**

|        | Oscilloscope reading | Specification  | Pass/Fail |
|--------|----------------------|----------------|-----------|
| E4837A |                      | Set1:<br><37mV | P / F     |
|        |                      | Set2:<br><42mV | P / F     |
| E4844A |                      | Set1:<br><37mV | P / F     |
|        |                      | Set2:<br><42mV | P / F     |
| E4845A |                      | Set1:<br><37mV | P / F     |
|        |                      | Set2:<br><42mV | P / F     |
| E4847A |                      | Set1:<br><37mV | P / F     |
|        |                      | Set2:<br><42mV | P / F     |